AMENDMENTS TO THE CLAIMS

1-11. (Canceled)

12. (Currently amended) ~~The method of claim 11~~ A method for suppressing carrier feedthrough in a quadrature transceiver, the method comprising:

performing a first search to determine a pair of receiver path correction signals;

performing a second search to determine a pair of transmitter path correction signals; and

using the pairs of receiver path and transmitter path correction signals to suppress carrier feedthrough in the quadrature transceiver, where using the pairs of receiver path and transmitter path correction signals comprises:

subtracting a first receiver path correction signal from a first downconverter output signal;

subtracting a second receiver path correction signal from a second downconverter output signal;

subtracting a first transmitter path correction signal from a first quadrature modulator ~~upconverter input~~ signal being input into an upconverter; and

subtracting a second transmitter path correction signal from a second quadrature modulator ~~upconverter input~~ signal being input into the upconverter.

13. (Currently amended) ~~The method of claim 11~~ A method for suppressing carrier feedthrough in a quadrature transceiver, the method comprising:

performing a first search to determine a pair of receiver path correction signals;

performing a second search to determine a pair of transmitter path correction signals; and

using the pairs of receiver path and transmitter path correction signals to suppress carrier feedthrough in the quadrature transceiver, where performing at least one of the first and second searches includes performing an algorithm selected from the group consisting of: a rotated binary search, an unrotated binary search, and a hybrid search.

14. (Currently amended) The method of claim 12 [[11]], further comprising operating the quadrature transceiver ~~modulator~~ in full-duplex mode.

15. (Currently amended) A program storage device, readable by a machine and tangibly embodying a representation of a program of instructions adapted to be executed by said machine to perform the method of claim 12 [[11]].

16. (Currently amended) A method for suppressing carrier feedthrough in a quadrature transceiver ~~modulator~~ comprising a transmitter path and a receiver path, the method comprising:

performing, during a first mode of operation, a first calibration to determine a first and second ~~pair of~~ receiver path correction signals;

performing, during a second mode of operation following the first mode of operation, a second calibration to determine a first and second ~~pair of~~ transmitter path correction signals using the receiver path of the quadrature transceiver ~~modulator~~; and

using, during a third mode of operation following the second mode of operation, the pairs of the receiver path and transmitter path correction signals to suppress carrier feedthrough in the quadrature transceiver ~~modulator~~.

17. (Currently amended) The method of claim 16, where using the pairs of the receiver path and transmitter path correction signals comprises:

subtracting the [[a]] first receiver path correction signal from a first downconverter output signal;

subtracting the [[a]] second receiver path correction signal from a second downconverter output signal;

subtracting the [[a]] first transmitter path correction signal from a first quadrature modulator ~~upconverter input~~ signal being input into an upconverter; and

subtracting the [[a]] second transmitter path correction signal from a second first quadrature modulator ~~upconverter input~~ signal being input into the upconverter.

18. (Previously presented) The method of claim 16, where performing at least one of the first and second calibrations includes performing a feedback DC calibration.

19. (Previously presented) The method of claim 16, where performing at least one of the first and second calibrations includes performing a binary search.

20. (Currently amended) The method of claim 16, further comprising operating the quadrature transceiver ~~modulator~~ in full-duplex mode.

21. (Previously presented) A program storage device, readable by a machine and tangibly embodying a representation of a program of instructions adapted to be executed by said machine to perform the method of claim 16.

22. (Currently amended) An apparatus for suppressing carrier feedthrough in a quadrature transceiver ~~modulator~~, the apparatus comprising:

a first pair of summers;

a quadrature modulator and an upconverter circuit coupled to the first pair of summers, each of the first pair of summers being operable to add ~~coupled to~~ [[a]] one of the outputs ~~first quadrature channel~~ of the quadrature modulator to one of a pair of transmitter path correction signals;

a multiplexer coupled to the upconverter circuit, to a ground, and to an RF front end;

a downconverter circuit coupled to the multiplexer;

a second pair of summers coupled to the downconverter circuit, each of the second pair of summers being operable to add ~~coupled to~~ [[a]] one of the outputs ~~second quadrature channel~~ of the downconverter ~~quadrature modulator~~ to one of a pair of receiver path correction signals; and

a correction circuit coupled to the first and second pairs of summers, the correction circuit performing a first correction method to determine the [[a]] pair of receiver path correction signals, and performing a second correction method to determine the [[a]] pair of transmitter path correction signals, and using the pairs of receiver path and transmitter path correction signals to suppress carrier feedthrough in the quadrature transceiver ~~modulator~~.

23. (Currently amended) The apparatus of claim 22, the correction circuit comprising:
a pair of averaging circuits coupled to the second ~~first~~ pair of summers;
a pair of absolute value circuits coupled to the pair of averaging circuits;
a summer coupled to the pair of absolute value circuits; and
a search circuit coupled to the summer.

24. (Previously presented) The apparatus of claim 23, the search circuit comprising a binary search circuit.

25. (Previously presented) The apparatus of claim 23, further comprising a feedback DC calibration circuit coupled to the pair of averaging circuits.

26. (Original) The apparatus of claim 22, further comprising a control circuit coupled to the correction circuit and to the multiplexer.

27. (Previously presented) The apparatus of claim 26, further comprising a program storage device coupled to the control circuit.

28. (Currently amended) An integrated circuit for suppressing carrier feedthrough in the quadrature transceiver ~~modulator~~ comprising the apparatus of claim 22.

29. (Currently amended) ~~The method of claim 11~~ A method for suppressing carrier feedthrough in a quadrature transceiver, the method comprising:
performing a first search to determine a pair of receiver path correction signals;
performing a second search to determine a pair of transmitter path correction signals; and
using the pairs of receiver path and transmitter path correction signals to suppress carrier feedthrough in the quadrature transceiver, where the first and second searches use a [[the]] same algorithm.

30. (Currently amended) The method of claim 16, where the first and second calibrations use a ~~the~~ same algorithm.